ISBN: 978-3-95450-227-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2022-TUPOST019

EVALUATION OF PIP-II MASTER OSCILLATOR COMPONENTS *

I. Rutkowski †, K. Czuba, A. Šerlat , Warsaw University of Technology, Warsaw, Poland
B. E. Chase, E. Cullerton, Fermi National Accelerator Laboratory/PIP-II, Batavia, Illinois, USA

Abstract

The Proton Improvement Plan-II (PIP-II) is a planned proton facility at Fermilab. The short- and long-term beam energy stabilization requirements necessitate using a high-quality Master Oscillator (MO). The consecutive sections of the Linac will operate at 162.5, 325, and 650 MHz. The phase relations between reference signals of harmonic frequencies should be kept constant, and the phase noise should be correlated in a wide bandwidth. The possibility of simultaneously meeting both requirements using popular frequency synthesis schemes is discussed. The ultra-low noise floor of the fundamental source is challenging for other devices in the phase reference distribution system. Therefore, the sensitivity to operating conditions, including impedance matching, input power level, and power supply voltage, must be considered. This paper presents a preliminary performance test of critical components selected for the PIP-II Master Oscillator system performed using a state-of-the-art phase noise analyzer.

INTRODUCTION

The Proton Improvement Plan II (PIP-II) is a plan of enhancement to the Fermi National Accelerator Laboratory (Fermilab) accelerator complex [1], the key component which is a 800 MeV superconducting radio-frequency linear accelerator made up of three consecutive sections operating at 162.5, 325, and 650 MHz. In addition, 1.3 GHz signal is needed to generate the high speed FPGA clock and a feedback for the phase reference line. The short- and long-term beam energy stabilization requirements necessitate using a high-quality Master Oscillator (MO). The reference generation will be combined with the distribution system to minimize the number of components. The MO will produce the lowest operating frequency, and harmonics will be generated at the beginning of a corresponding section.

The phase relations between reference signals of harmonic frequencies should be kept constant, and the phase noise should be correlated in a wide band (1 MHz or more). With these two aspects in mind, we will investigate the main classes of synthesizers:

- indirect digital,
- direct digital,
- direct analog.

An indirect digital synthesizer utilizes a Phase Lock Loop (PLL) with an integer or fractional frequency divider. The loop bandwidth is limited (typically below one hundred kHz) due to the high gain of a low phase noise VCO and insufficient phase margin. The phase relation is maintained constant by the loop.

A direct digital synthesizer (DDS) uses a numerically controlled oscillator feeding a digital-to-analog converter, both synchronized by the same clock. Without increasing the input clock internally (typically using an additional PLL), a DDS can not generate an output signal of a frequency higher than the reference. This limitation renders it unsuitable for this application.

The direct analog approach uses frequency dividers, mixers, and filters to produce and select the desired spectral component at the mixer's output. Within the band-pass, the device closely follows the PN of the reference, with the additional noise induced by the optional divider and the mixer.

In the direct methods, there is no loop guaranteeing the phase relations.

In all three aforementioned methods, the frequency ratio ($\frac{f_{out}}{f_{in}}$) can be fractional. If the allowed ratios are limited to natural values (in this application, this limitation is not prohibitive), other techniques can be employed. Non-linear elements like step recovery diodes generate a train of very fast pulses occurring one every cycle of the input signal. A notch filter selects the desired harmonic. The noise correlation bandwidth is determined by the filter (making it easy to obtain a wide bandwidth), but the phase relation is not guaranteed.

No architecture simultaneously fulfills both requirements. Since the phase can be stabilized with an auxiliary circuit, the harmonic generation technique was selected as it can provide the lowest residual noise.

Fermilab and Warsaw University of Technology (WUT) are collaborating on the design of the MO and the phase reference line for PIP-II. In the following sections, the measurement results of the proposed MO and frequency multipliers are presented. Unless otherwise noted, the measurements were performed at WUT in a Faraday cage using a Rhode & Schwarz FSWP phase noise analyzer. The jitter will be given as an integral in the 10 Hz to 1 MHz band.

MASTER OSCILLATOR

A vibration isolated narrow-band voltage controlled oscillator generating 10 MHz and 162.5 MHz output signals was custom-made by Wenzel for the linac. Figure 1 shows the measured phase noise spectra of both signals as well as the calculated spectrum of the 10 MHz signal perfectly

* The paper was prepared by Warsaw University of Technology and Fermi National Accelerator Laboratory/PIP-II, using the resources of Fermi National Accelerator Laboratory (Fermilab), a U.S. Department of Energy, Office of Science, HEP User Facility. Fermilab is managed by Fermi Research Alliance, LLC (FRA), acting under Contract No. DE-AC02-07CH11359.
Research was funded by POB HEP of Warsaw University of Technology within the Excellence Initiative: Research University (IDUB) programme.
† Igor.Rutkowski@pw.edu.pl

ISBN: 978-3-95450-227-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2022-TUPOST019

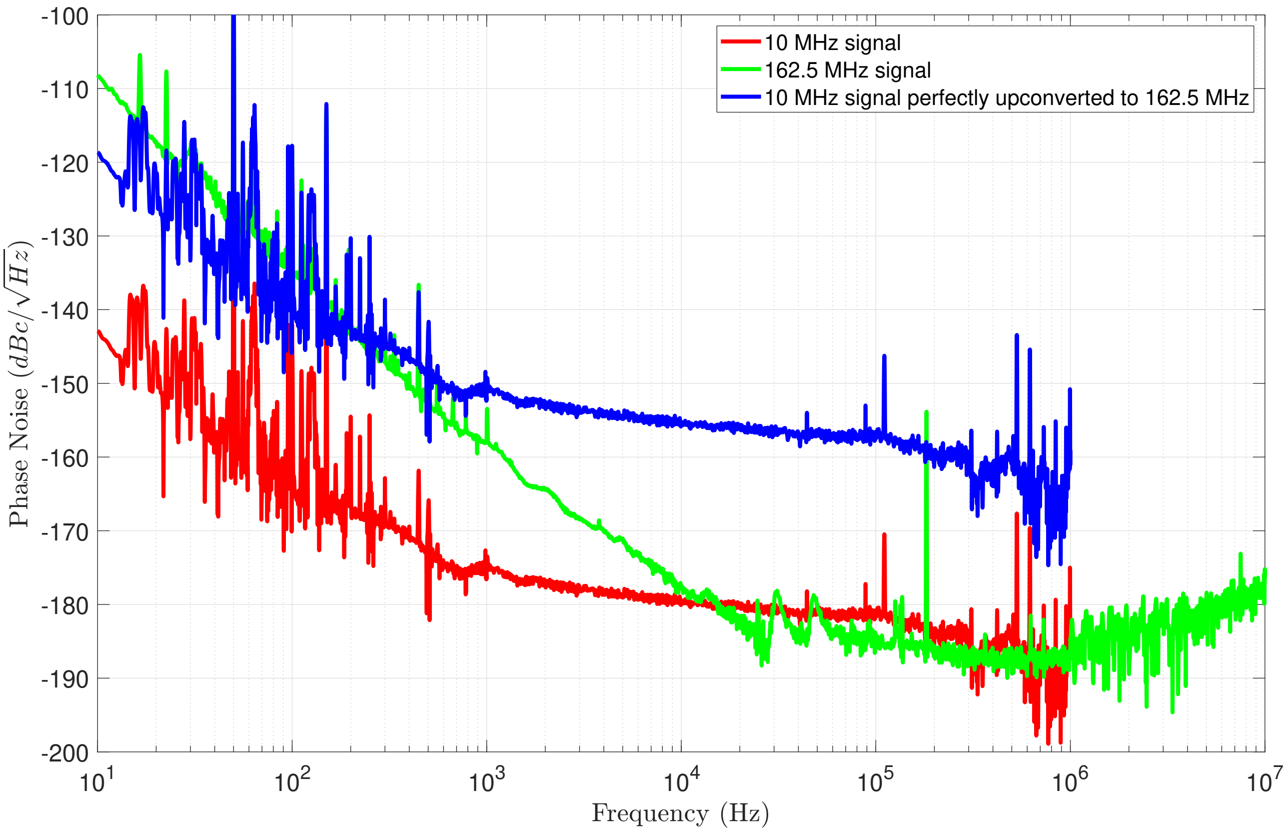

Figure 1: Phase noise spectra of 10 MHz and 162.5 MHz signal at the ouptut of a vibration isolated narrow-band voltage controlled oscillator made by Wenzel. For comparison, the low frequency trace was perfectly translated to the higher frequency.

up-converted to 162.5 MHz. The VCO was free-running, with tuning input grounded. The two signals are locked up to around 200 Hz (the frequency at which the up-converted and high-frequency traces cross). Up to 10 dB of 1/f noise is added to the 162.5 MHz signal within the locking bandwidth. This noise slope goes down to below -180 dBc/Hz when it crosses with white noise. The jitter of the signals equals 23.60 fs and 22.90 fs (10 MHz and 162.5 MHz, respectively). The source of the spur at 180 kHz was not determined.

First measurements were performed using Agilent E5052B Signal Source Analyzer (see Fig. 2). The results differ either because of the instrument's limited sensitivity or different loading of the filter at the MO output.

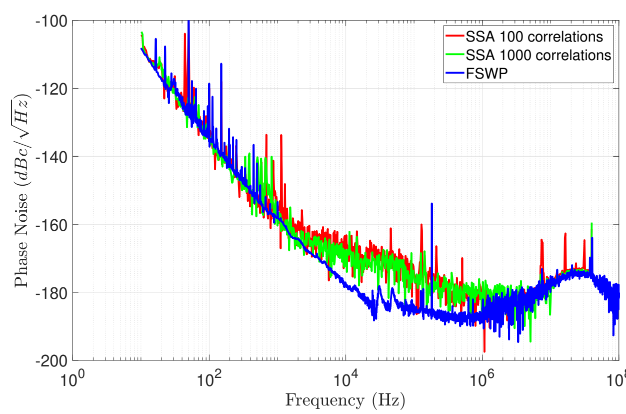

Figure 2: Phase noise spectra of measured frequency multipliers normalized to the highest frequency (1300 MHz).

FREQUENCY DOUBLERS

Wenzel's Integrated Frequency Multipliers (IFM) 1R series of devices was selected for evaluation based on:

- multiplication factor
- integrated filters
- integrated amplifiers
- output power
- residual phase noise level

Figure 3 shows the measured phase noise spectra of all signals, which were all normalized to the highest frequency (1300 MHz). The devices add very little noise below 10 kHz. The noise floor is raised by around 10 dB by the first stage, 2 dB by the second, and less than a dB by the last stage. The significant increase in the 10 kHz - 1 MHz bands translates to a minor rise in the total jitter, which equals 21.35, 23.82, and 23.88 fs. The first result is smaller than the reference, which can be attributed to measurement error.

ISBN: 978-3-95450-227-1 ISSN: 2673-5490 doi:10.18429/JACoW-IPAC2022-TUPOST019

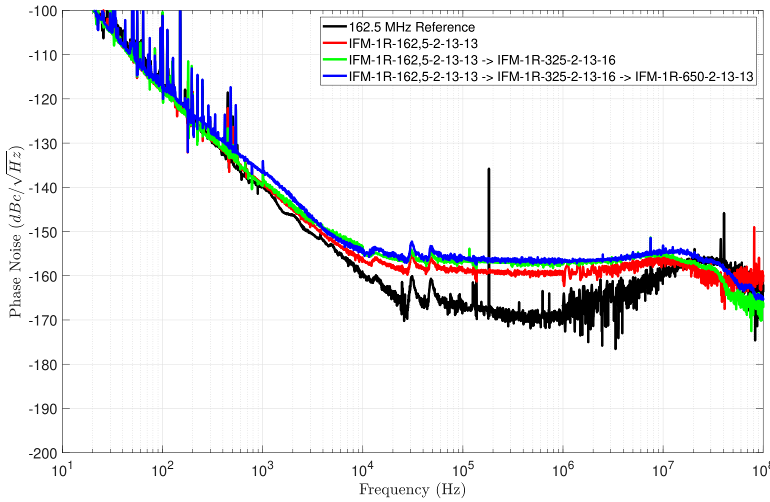

Figure 3: Phase noise spectra of measured frequency multipliers normalized to the highest frequency (1300 MHz).

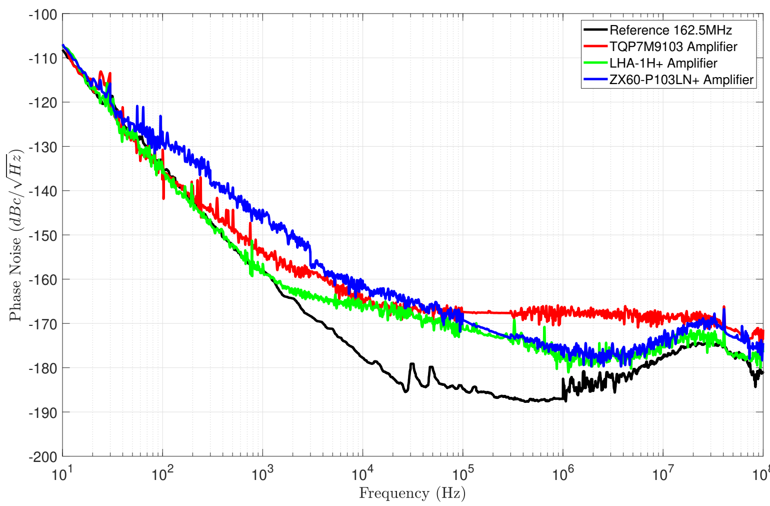

Figure 4: Amplifiers' phase noise comparison.

AMPLIFIERS

Although the source and the active frequency multipliers have output power levels above +10 dBm, the signals must be amplified due to losses in cabling and circuits. Three models were tested:

- TQP7M9103 from Qorvo (1W High Linearity Amplifier),
- LHA-1H+ from Mini-Circuits (Ultra High Dynamic Range Monolithic Amplifier, max P1dB at +22.7 dBm), and
- ZX60-P103LN+ from Mini-Circuits (Low Noise Amplifier, max P1dB at 23.8 dBm).

Figure 4 shows the measured phase noise spectra of signals at the output of each device fed with the MO reference signal. The input power level was adjusted (individually for each amplifier) to minimize the jitter. All devices add residual 1/f and white noise, which is 20 dB above the input level in the worst case. However, this does not translate to a significant increase in the integrated jitter, which equals 22.69, 23.93, and 19.72 fs.

CONCLUSIONS

The selected MO provided a very high-quality signal. Its phase noise in the 30 kHz - 5 MHz band is so low that all other devices in the chain (amplifiers and frequency multipliers) add 10 to 20 dB of white noise, which still only insignificantly rises the total jitter.

REFERENCES

[1] A. Saini, E. Pozdeyev, and V. P. Yakovlev, "The Beam Dynamics Updates of the Fermilab PIP-II 800 MeV Superconducting Linac", in *Proc. 19th Int. Conf. RF Superconductivity (SRF'19)*, Dresden, Germany, Jun.-Jul. 2019, pp. 123–126. doi:10.18429/JACoW-SRF2019-MOP033