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PEG CONTRIBUTION TO THE LLRF SYSTEM FOR SUPERCONDUCTING ELLIPTICAL CAVITIES OF ESS ACCELERATOR LINAC*

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Abstract

The LLRF (Low-Level Radio Frequency) system optimizes energy transfer from the superconducting resonator to the accelerating beam. At ESS, one LLRF system regulates a single cavity. This digital system's hardware platform is the MTCA.4 standard. The system has been co-designed by ESS, Lund University, and the PEG (Polish Electronic Group) consortium. The PEG is also responsible for the system components design, evaluation, and production (like Local Oscillator Rear transition module, piezo tuner driver RTM, RTM carrier board, and others). The PEG delivers a hardware/software cavity simulator, an LLRF system test-stand, and provides necessary integration and installation services required for complete system preparation for the linac commissioning and operation phase. The paper summarizes the PEG work on the development and preparation of the LLRF systems for the ESS elliptical structures. The efforts concerning hardware and software components prototyping and evaluation are discussed. Moreover, we present the current status of the project, including components mass production, integration, and installation work.

INTRODUCTION - LLRF SYSTEMS FOR ESS ELLIPTICAL RESONATORS

The Low-Level Radio Frequency (LLRF) control system's primary goal is to provide optimal energy transfer from the cavity to the accelerated particles beam.

The ESS project foresees a single cavity regulation scheme (see Fig. 1). The presented diagram describes the system setup for spokes and elliptical cavities. But the general idea was the unification of different system types. The MTCA.4 [1] standard provides enough versatility by means of dedicated sub-modules configuration ability for given system kind. The set-up of the controller comprises of different hardware modules [3]. Some of them were designed and delivered by PEG (RTM carrier, LO-RTM, Piezo driver). The consortia members responsibility includes also LLRF system integration and installation at the ESS linac side. The elliptical cavity simulator and complete system loop test-stand enabled reliable verification of the LLRF system components and set-up.

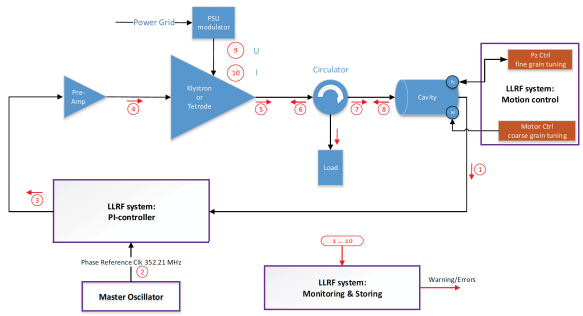

Figure 1: Overview of the LLRF system [2].

MTCA.4 HARDWARE MODULES DESIGNED BY PEG

RTM Carrier AMC Module

The RTM Carrier (Fig. 2) is low cost FPGA based MTCA.4 AMC module, dedicated for supporting LO RTM (Fig. 3) and Piezo RTM (Fig. 4) boards in the LLRF systems. Board is equipped in Artix-7 FPGA device, it has also 1GB of DDR3 memory and covers PCIe x2 and Low latency Links (direct board-to-board connections) on the MTCA backplane. In the LLRF system architecture, the RTM Carrier board provides minimal functionality that allows RTMs to operate. The general required functionality of the board is: communication with the RTM via ZONE 3, powering RTM devices, communication with the other devices using PCI-Express on the backplane, data processing in the FPGA, fulfilling all the other requirements for the AMC board defined in the MTCA.4 standard.

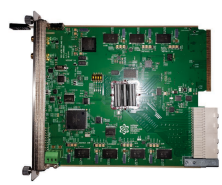

Figure 2: RTM Carrier AMC module.

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Local Oscillator RTM Module

The LO Rear Transition Module (LO RTM) generates and distributes clock ($f_{ref}/6$ = 117.403 MHz) and LO (f_{ref} * 23/22 = 736.439 MHz or f_{ref}*29/28 = 729.578 MHz) signals synchronous to an externally fed 704.42 MHz reference. To follow the input phase noise in wide offset bandwidth, the clock signal is generated by a frequency divider and the LO using a frequency divider, mixer, and band-pass filter (direct analog scheme). The signal conditioning path includes amplifiers, alternators, and power dividers.

The LO RTM communicates with an AMC via the Zone3 connector. The AMC can set the board parameters (enable/disable the clock signal, enable/disable the LO signal, select the IF, configure the attenuation, and others) as well as read out the input and output powers.

Long-term tests of Revision 1.2 (see Fig. 3) validated the design.

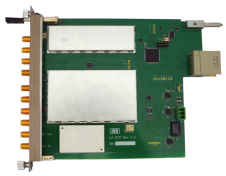

Figure 3: Photo of the LO RTM Revision 1.2.

Piezo Driver RTM Module and Power Supply

The PEG group delivers the hardware module [4], which the main purpose is to provide a command signal to the resonators' fine tuners. The solution comprises two major components. One is the RTM (Rear Transition Module) format board (MTCA.4 standard) that handles high voltage control signal waveforms generation and signals monitoring (acquisition) named HPD-200 (see Fig. 4). Other component is an external power supply unit that delivers necessary HV to the HPD-200 module. The RTM module paired with

Figure 4: Photo of the Piezo RTM Revision 2.1.

the AMC RTM carrier board provides all required functionalities for piezo operation and diagnostics. The piezo driver controller can generate the DC voltage and AC components and pre-defined customized wave-forms shapes of the signal.

System configuration allows for work with different cavity types. While M-Beta and H-Beta elliptical cavities accept uni-polar excitation ranging from 0 to 200 V, the spoke ones can operate -40V to 160 V. Considering cavities dynamics, we have specified that piezo driver should be able to work with up to 1 kHz bandwidth to cover desired tuning control needs.

Tests performed on the local dedicated test stand and all types of the prototype cavities (spokes, M-Beta and H-Beta) allowed for tailoring the design and device performance to the system owners' needs.

CAVITY SIMULATOR

Cavity Simulator [5] (see Fig. 5) was designed to help the LLRF developers to test their system before connecting it to the actual equipment. This device simulates the behavior of the superconducting cavity used at medium and high beta sections of the ESS linac. The simulated phenomena include cavity dynamics, piezo detuning, and beam current. The model of the amplifier is also included in the simulation scope.

The device is based on a high-performance FPGA with a set of data converters and a dedicated RF frontend. In total, it consists of seven modules. Six of those were designed internally by the Institute of Electronic Systems. The input signals from the LLRF control system are digitized. Those signals are then processed inside the FPGA firmware, and the responses are generated and converted through DAC to analog and RF signals.

Figure 5: Photo of the cavity simulator front panel.

TEST STAND

The PEG established local LLRF hardware and software test stand for system integration and particular sub-modules verification. The consortium delivers various HW and SW modules tested individually. Still, testing of the integrated system with conditions similar to regular operation is essential to correctness and performance determination. Availability and configuration flexibility are significantly higher than the real (cryomodule) system option with lower operation cost. The test stand integrates the complete configuration of the LLRF related MTCA.4 modules in the single rack. Additionally, the control loop is closed via the cavity simulator that is paired with the LLRF part. The CS contains also the reference and clock signal generators, which make the test-stand fully standalone structure.

LLRF SYSTEM RELATED FIRMWARE

MTCA.4 Modules Firmware

The ESS delivers the firmware framework and the main accelerating field controller software implementation. The PEG handles the FW packages that comply with the framework guidelines. One is the board support package (BSP) for the RTM carrier board, that gives access to the module's major components and peripherals. Other is the LO-RTM dedicated FW assures access to the board registers, allowing for the clock (CLK) and LO signals configurations. Finally,

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the piezo driver FW enables configuration and management of the piezo channel modes (actuator or sensor). It also defines and provides interface to the memory used for the piezo excitation waveforms storage. It implements the acquisition channels that contain the data from the PD voltage and current output measurement, as well as the piezo signals.

MMC Firmware

The RTM carrier and Piezo-RTM modules (by PEG) are equipped with dedicated MMC processors. This allows for an IPMI functionality integration. The firmware developed for these controllers provided access to the various types of sensors (voltage, temperature, etc) present on the board and also other hardware information like Field-replaceable Unit (FRU) records. The latest MMC FW version integrates support for both AMC and RTM PEG modules.

OTHER HARDWARE MODULES

PSS Switch

The PSS Switch is a device to turn off the RF power going to Klystron if Personal Safety Systems detect an emergency. The device is based on an RF relay manufactured by Radial. The control signal comes directly from the PSS controller.

Pin Diode

The PIN-Diode module (Fig.6) is a fast RF-gate, which shall block the RF signal going from the LLRF system to the klystron, when the Machine Protection System (MPS) event occurs. Signal that indicates the RF-stop condition is delivered to the board using optical fiber. Special attention was paid to the behaviour of this device in case of power loss, to ensure that in such case there will be no signal transmission. The device has Ethernet interface which is used to query device status and allows MPS system testing.

Figure 6: PIN-Diode.

Electron Pick-up

The aim of the Electron-pickup is to measure the the current generated in the superconducting cavities due to the multipacting phenomenon. If this current exceeds provided threshold, an interlock signal is generated and transmitted using optical fiber interface to the MPS. In contrast to PIN-Diode, this board does not receives, but generates the the interlock signal.

Figure 7: Electron pickup.

RF Splitbox

The RF Splitbox [6] is responsible for distributing the RF signal inside the LLRF racks (see Fig. 8). The device consists of 9 custom-designed power splitters optimized to achieve the lowest possible phase drifts and very low crosstalk between the channels. The device is manufactured in different versions for different parts of the ESS accelerator.

Figure 8: Photo of the RF Splitbox.

LLRF SYSTEMS INSTALLATION

The general procedure for LLRF system testing and installation includes following steps: assembly the MTCA crate in laboratory, test the crate in the laboratory with the cavity simulator (Fig. 5) - check if LLRF works (Factory Acceptance Test - FAT), install the crate in the klystron gallery, perform the inner rack cabling, repeat the crate test in the klystron gallery with the cavity simulator attached to the patch-panel on the top of the rack (Site Acceptance Test - SAT).

Due to various global circumstances, as of now, the installation of LLRF system has been delayed, only 8 LLRF system has been officially installed in February 2021. The subsequent installations has been postponed due to global market situation, especially in case of ordering electronic components, cables and other materials and devices.

SUMMARY

As of now, the PEG partners concluded the design and prototype phases for most components. Verification of the final design versions took place in the dedicated LLRF tests stand and in the accelerator environment with a single (M-Beta resonators) cryomodule facility.

For most of the HW module types, mass production took place. In the case of the RTM carrier and LO-RTM, they are ready for installation in the M-Beta dedicated systems. The piezo driver systems needed additional prototyping run because of the device specification change. The mass production process for the rest of the HW is ongoing and will finish by the end of 2022.

Integrated LLRFs are now in operation in different facilities at the PEG and ESS sides. The systems installation activities are ongoing in the klystron gallery hall of the linac - to be concluded by mid of 2023. This deadline may change depending on existing the global market situation related to the supply chain problems and semiconductor crisis.

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